

EAIDK310

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Bill of Materials

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note:

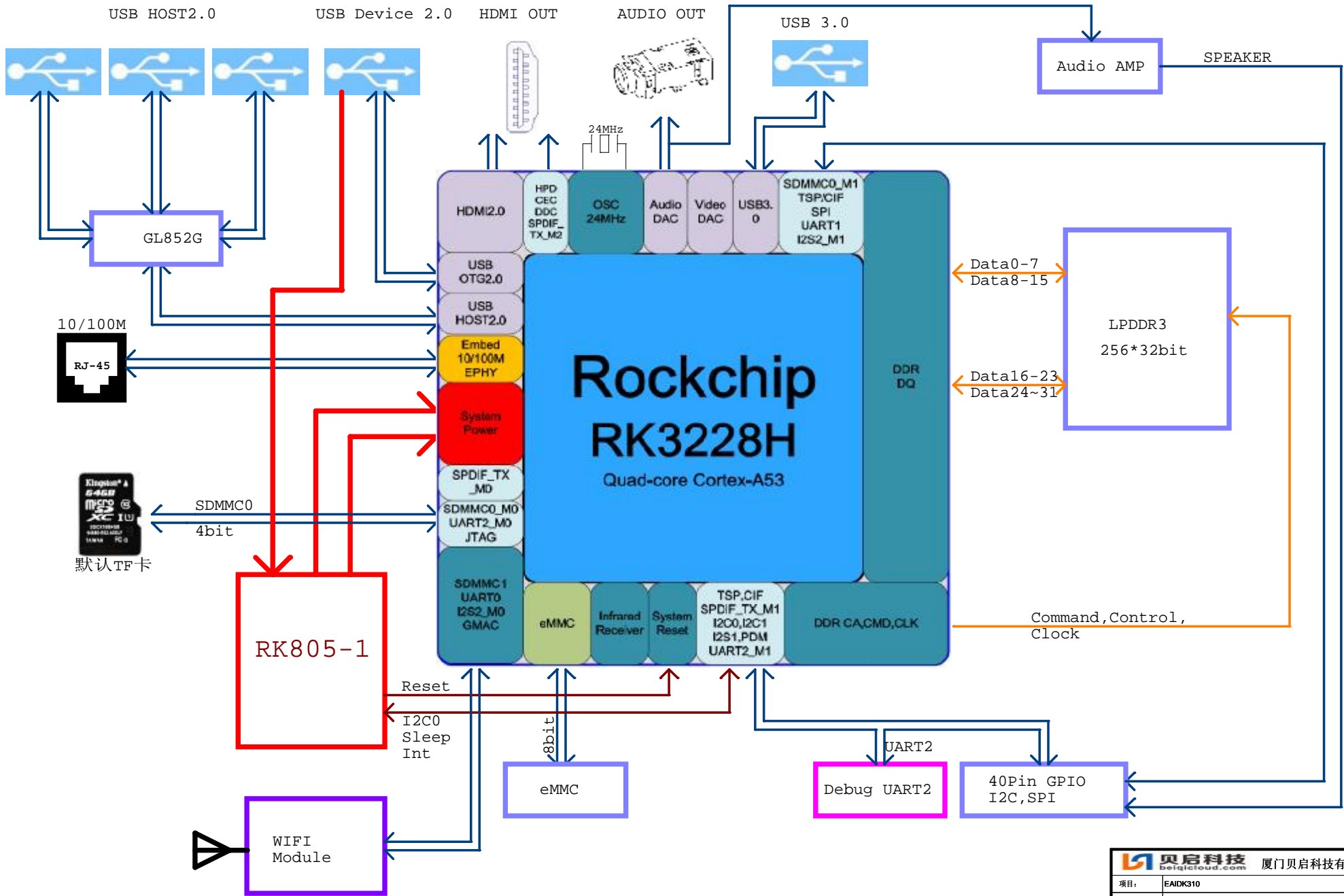
Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

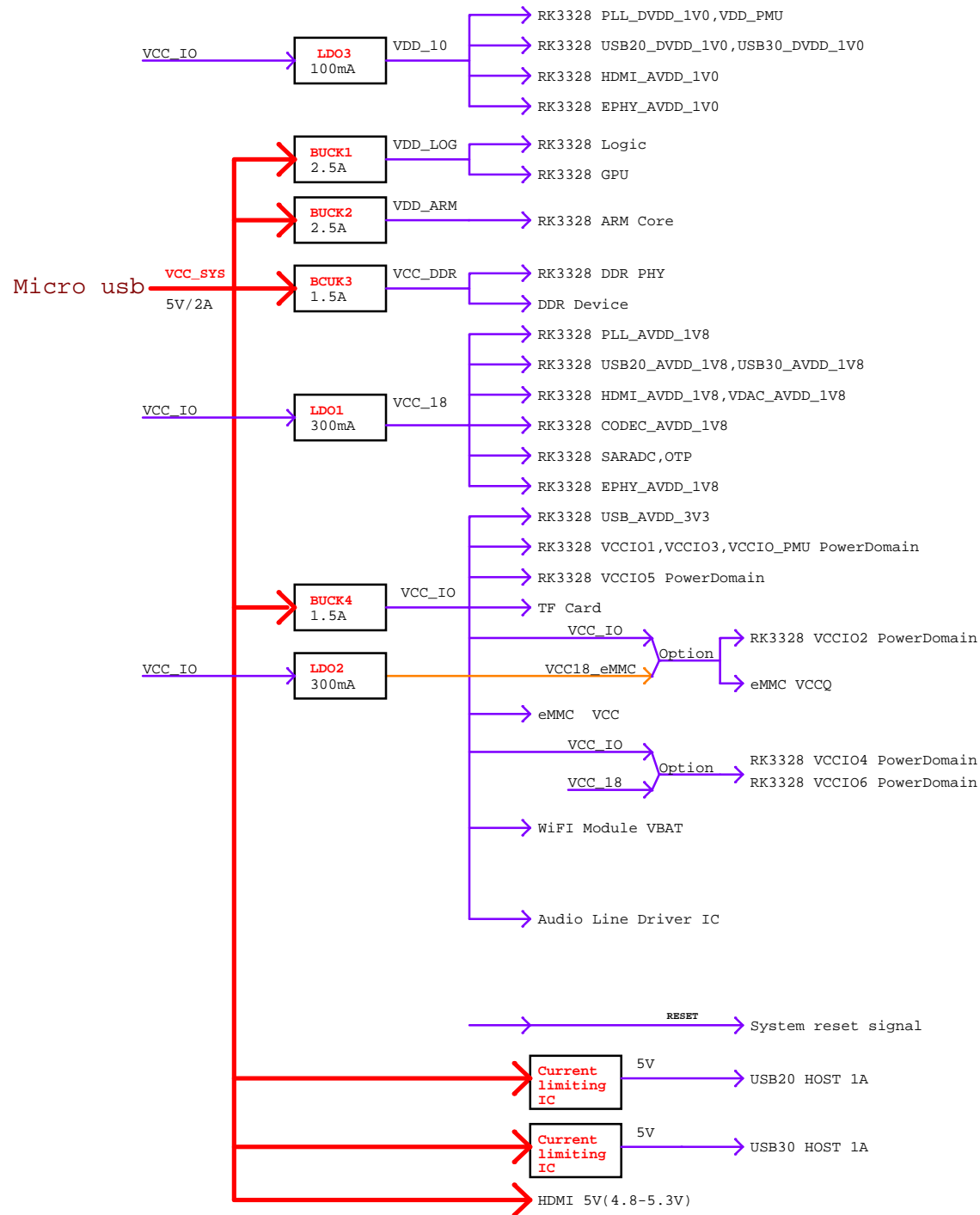
 厦门贝启科技有限公司	
项目:	EAIDK310
文件:	EAIDK310_MAINBOARD
图纸:	01.Index
修改日期:	Wednesday, May 08, 2019
版本:	V0.1
设计者:	CZA
页码:	1 of 22

Version	Date	Author	Change Note	Approved
v1.0	20190308	CZA	First edictor	

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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	02.Change List		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	2 of 22



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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	03.Block Diagram		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
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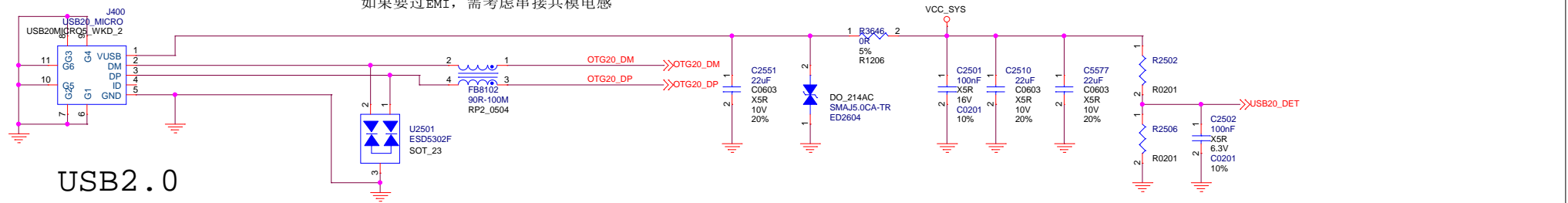
Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V	2	VDD_LOG
BUCK2	1.1V	2	VDD_ARM
BUCK3	FB=0.8V	3	VCC_DDR
BUCK4	3.3V	4	VCC_IO
LDO1	1.8V	4	VCC_18
LDO2	1.8V	4	VCC18_eMMC
LDO3	1.0V	4	VDD_10

IO电源域电压	IO电压=3.3V	IO电压=1.8V	
VCCIO_PMU	3.3V	不支持	
VCCIO1	3.3V (默认)		
VCCIO2		1.8V (默认)	eMMC
VCCIO3	3.3V (默认)	1.8V (SDIO3.0)	
VCCIO4		1.8V (默认)	SDIO3.0 for WIFI
VCCIO5	3.3V (默认)		
VCCIO6	3.3V (默认)		

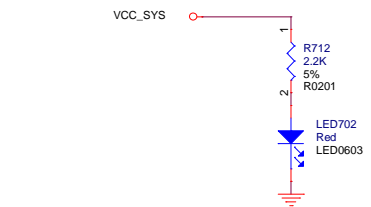


如果要过EMI, 需考虑串接共模电感



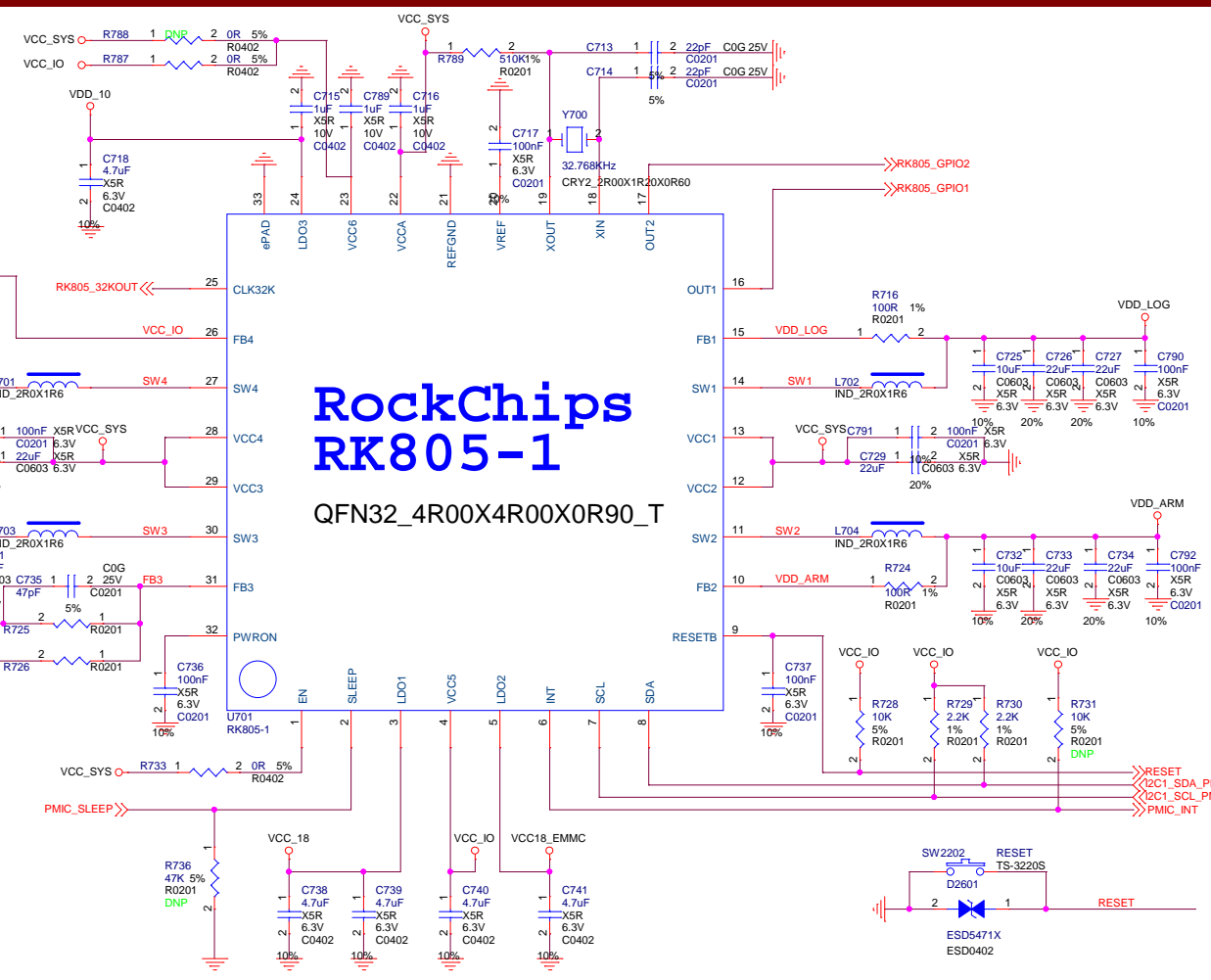
USB2.0

LED DISPLAY



RockChips RK805-1

QFN32_4R00X4R00X0R90_T



VCC_DDR

Default:DDR3=1.25V

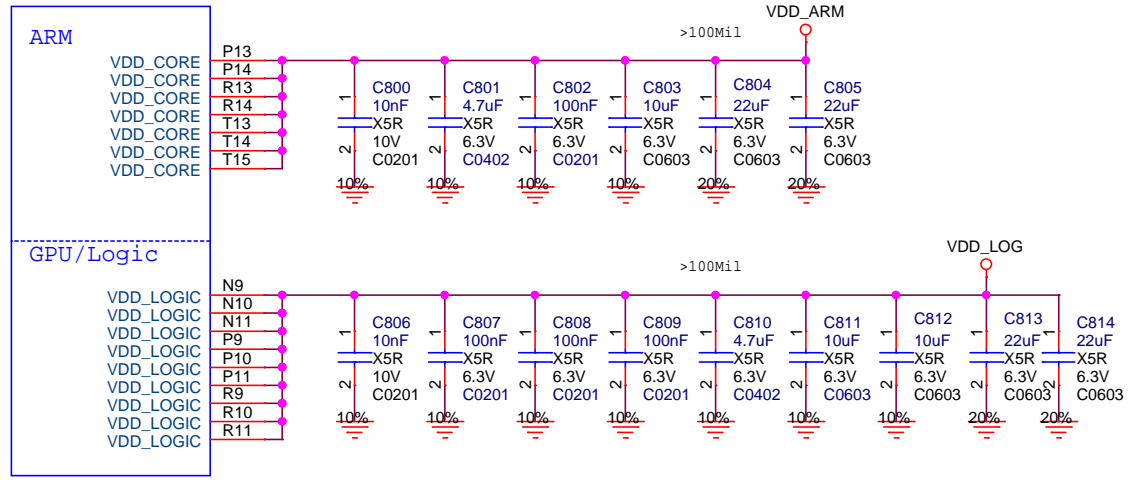
	DDR3	DDR3L	LPDDR3
VCC_DDR	1.527V	1.353V	1.25V
R725	100K 1%	47K 1%	68K 1%
R726	110K 1%	68K 1%	120K 1%

- M700 MARK
- M701 MARK
- M702 MARK
- M703 MARK
- M704 MARK
- M705 MARK

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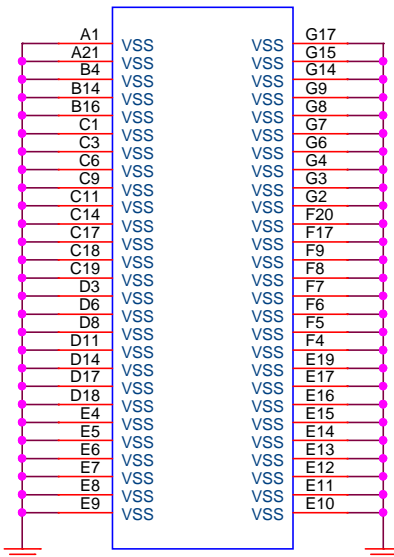
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文件:	EAIDK310_MAINBOARD		
图框:	05.System Power-PMIC RK805-1		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	5 of 22

U800N



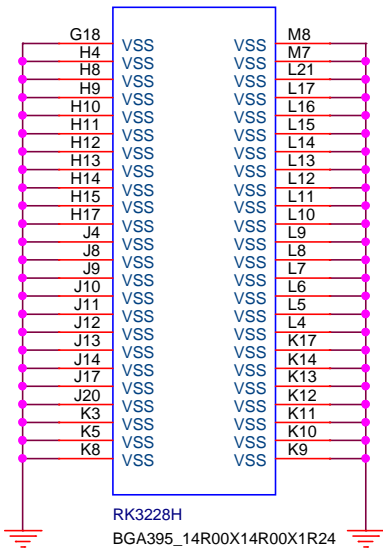
RK3228H
BGA395_14R00X14R00X1R24

U800O



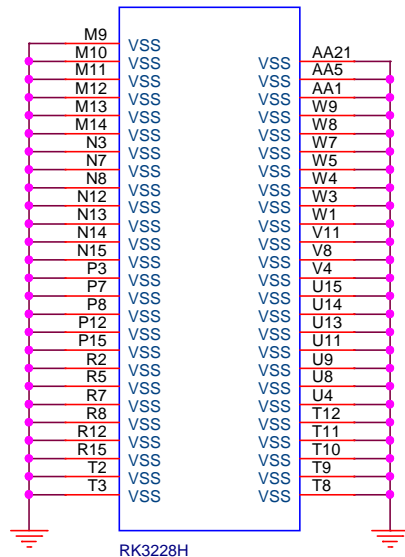
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U800P




RK3228H
BGA395_14R00X14R00X1R24

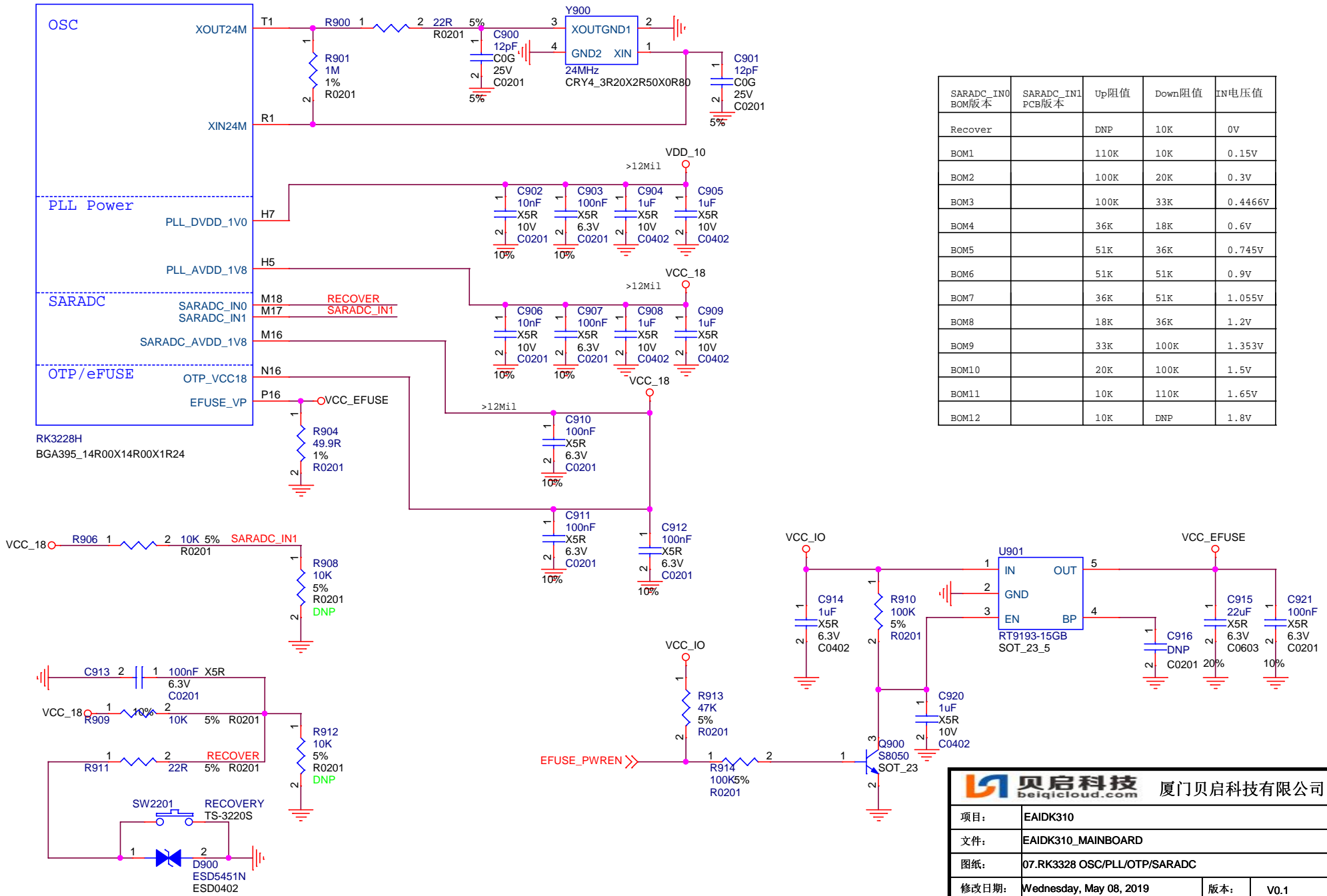
U800Q



RK3228H
BGA395_14R00X14R00X1R24

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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	06.RK3328 Power		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
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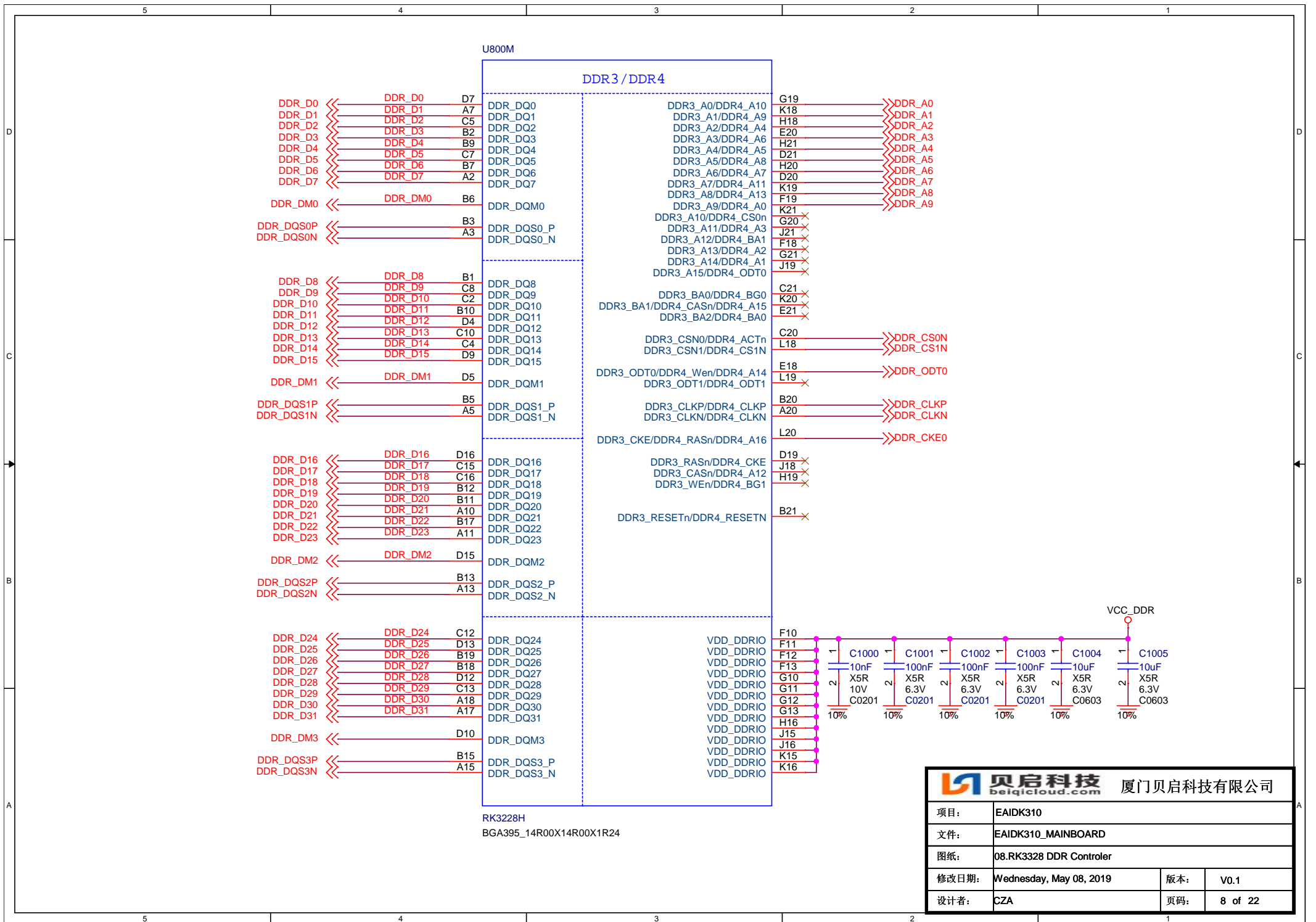
U800A



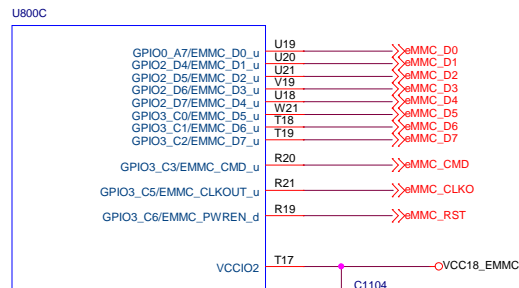
SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	IN电压值
Recover		DNP	10K	0V
BOM1		110K	10K	0.15V
BOM2		100K	20K	0.3V
BOM3		100K	33K	0.4466V
BOM4		36K	18K	0.6V
BOM5		51K	36K	0.745V
BOM6		51K	51K	0.9V
BOM7		36K	51K	1.055V
BOM8		18K	36K	1.2V
BOM9		33K	100K	1.353V
BOM10		20K	100K	1.5V
BOM11		10K	110K	1.65V
BOM12		10K	DNP	1.8V

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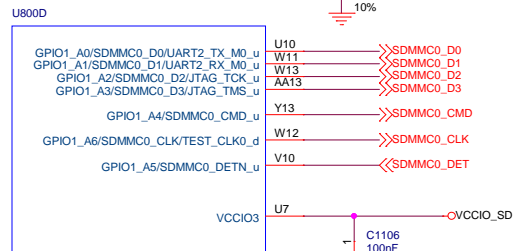
项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	07.RK3328 OSC/PLL/OTP/SARADC		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
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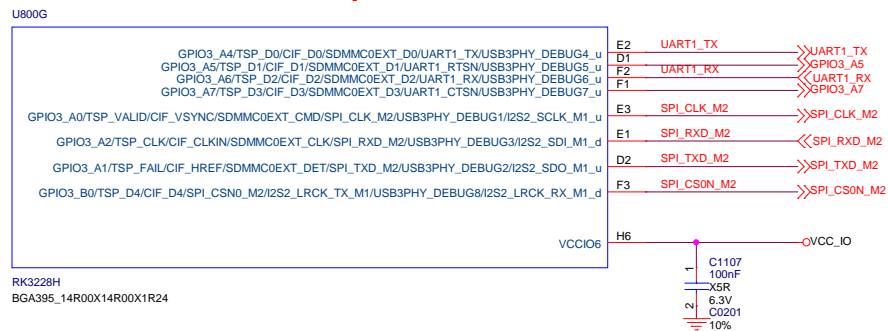
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文件:	EAIDK310_MAINBOARD		
图纸:	08.RK3328 DDR Controller		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
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RK3228H
BGA395_14R00X14R00X1R24

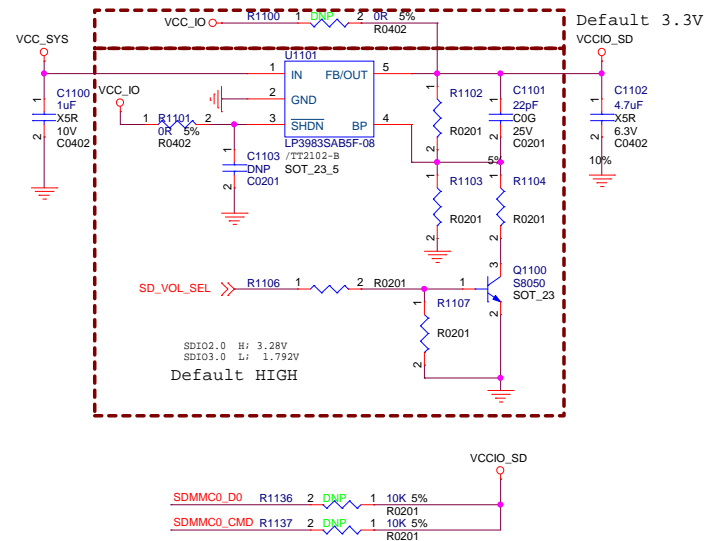


RK3228H
BGA395_14R00X14R00X1R24



RK3228H
BGA395_14R00X14R00X1R24

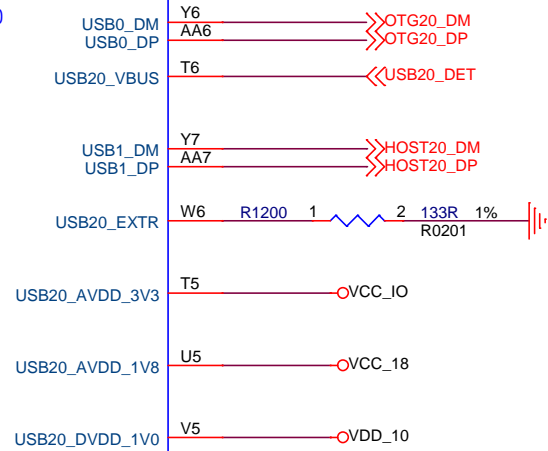
SDMMC0复用了两个位置，
同时只能用其中一个位置，
VCCIO3上的复用，可支持boot，
VCCIO6上的复用，不可支持boot。



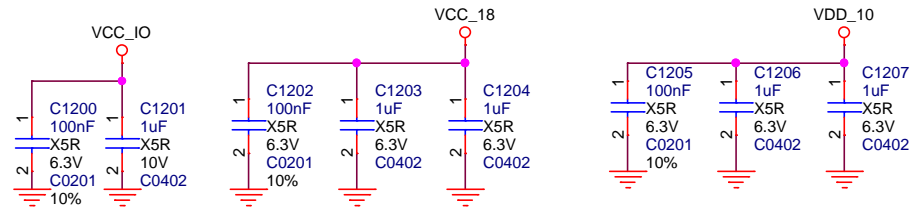
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项目:	EAIKD310
文件:	EAIKD310_MAINBOARD
图纸:	09.RK3328 FLASH Controller/TF
修改日期:	Wednesday, May 08, 2019
设计者:	CZA
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U800K

USB2.0

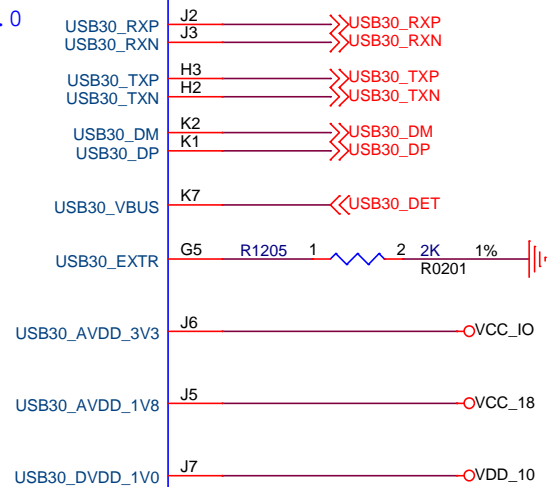


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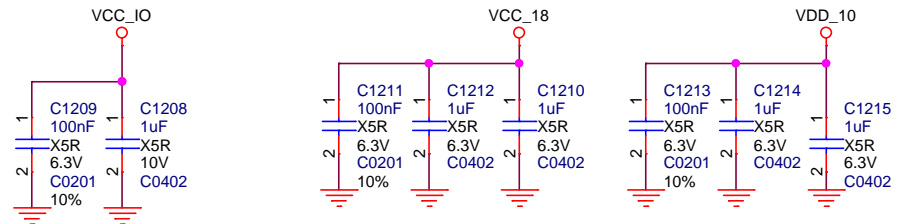


U800L

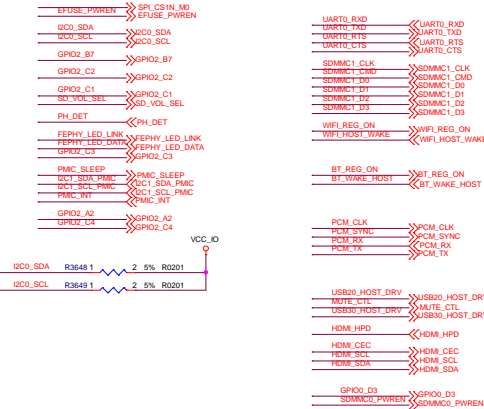
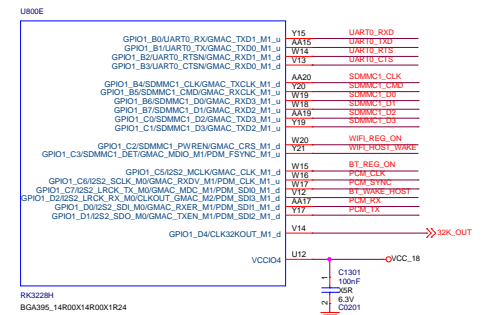
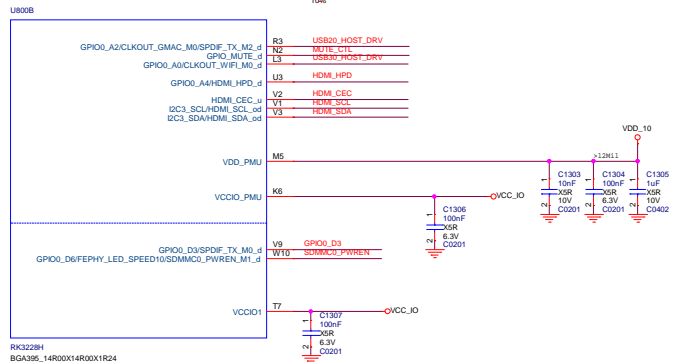
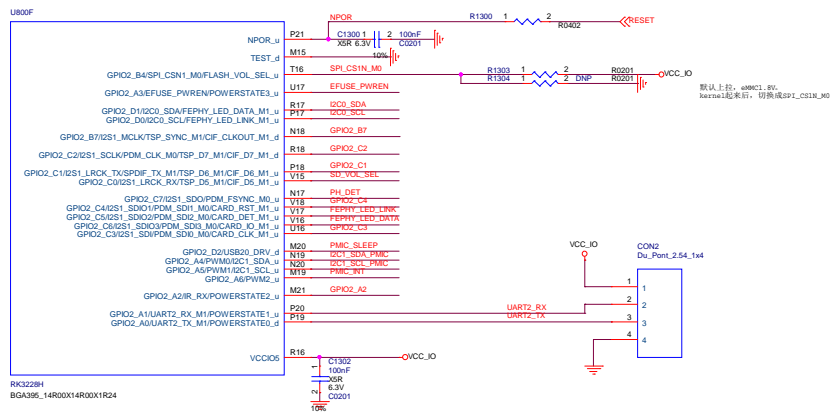
USB3.0



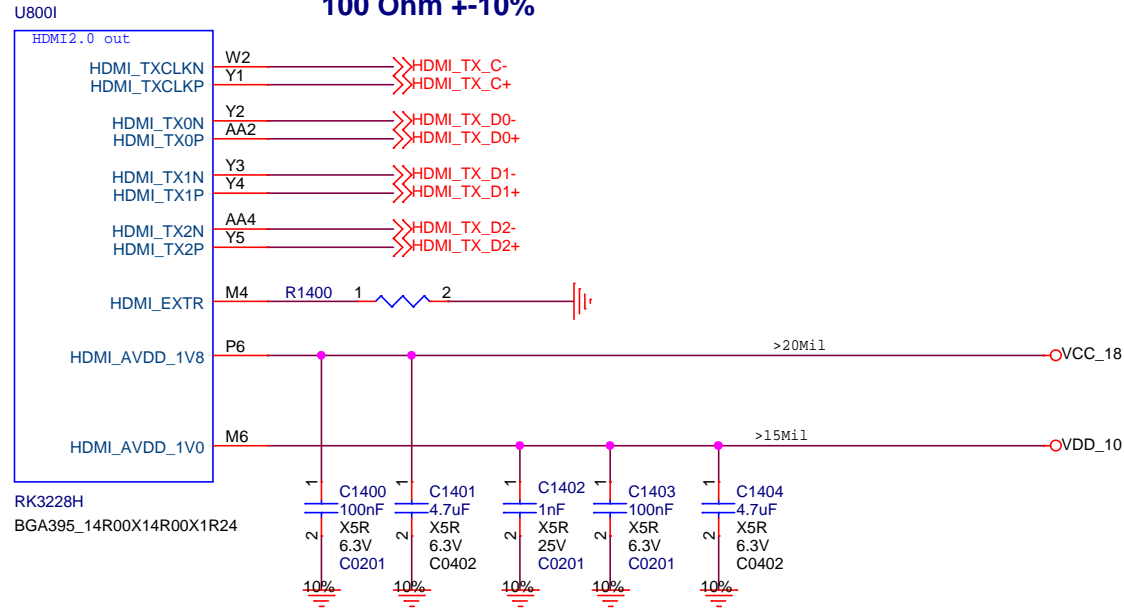
RK3228H
BGA395_14R00X14R00X1R24



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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	10.RK3328 USB2 PHY/USB3 PHY		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	10 of 22

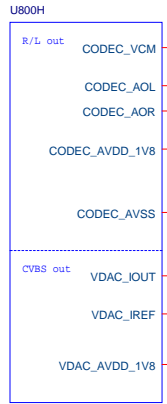


HDMI TMDs trace 100 Ohm \pm 10%

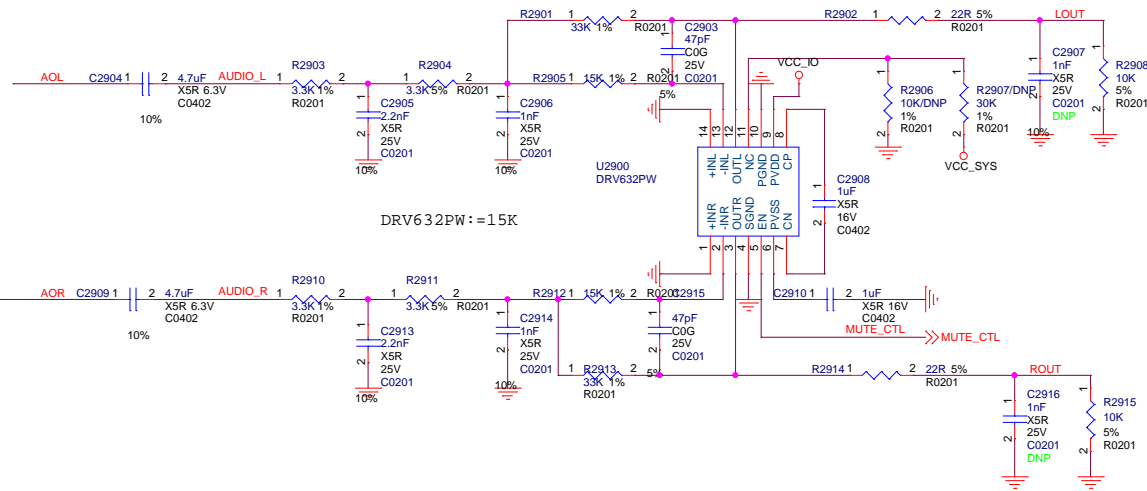
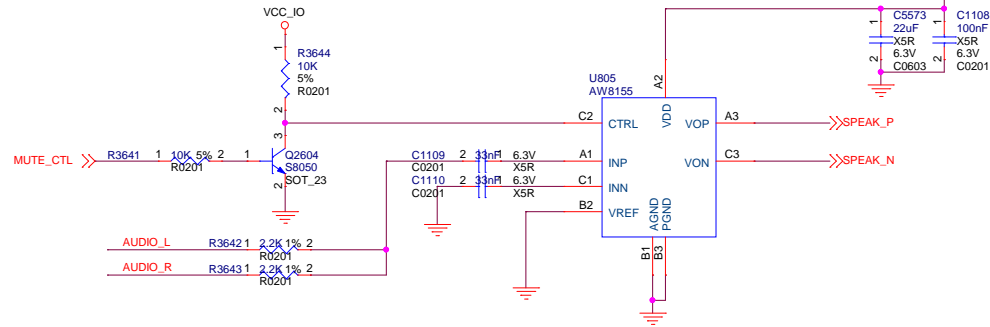
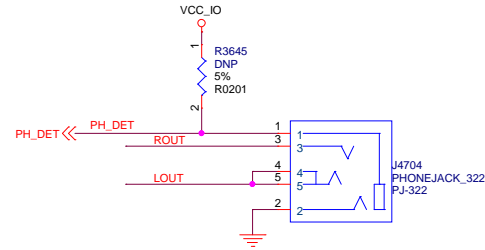


RK3228H
BGA395_14R00X14R00X1R24

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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	12.RK3328 HDMI PHY		
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设计者:	CZA	页码:	12 of 22



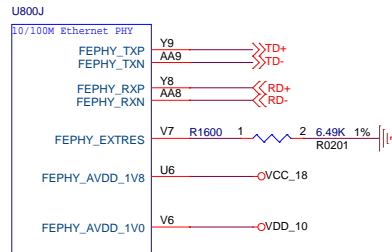
RK3228H
BGA395_14R00X14R00X1R24



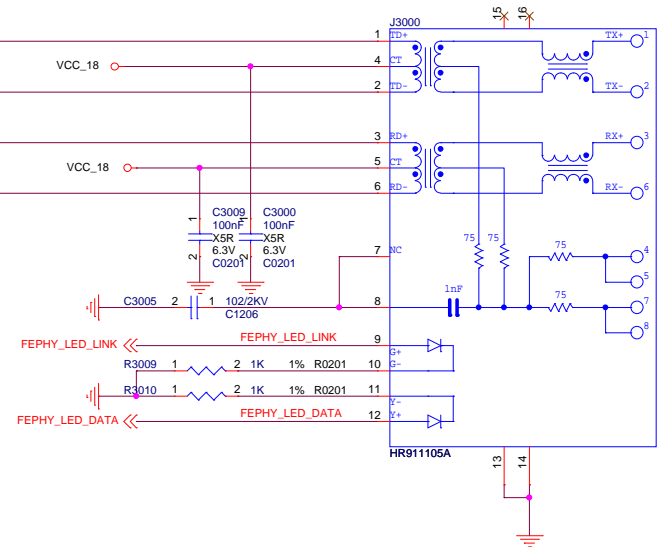
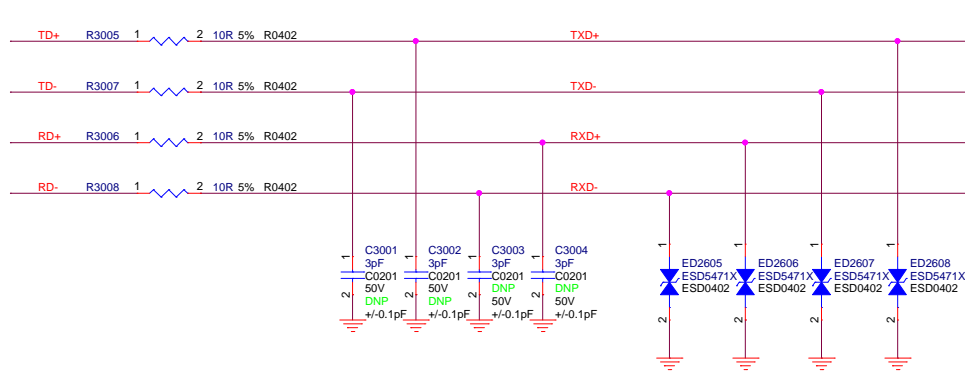
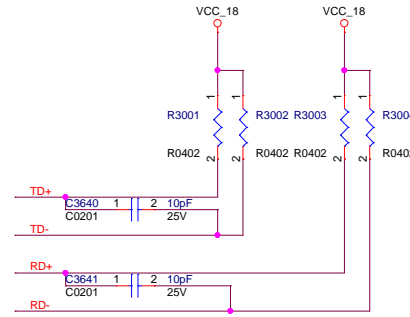
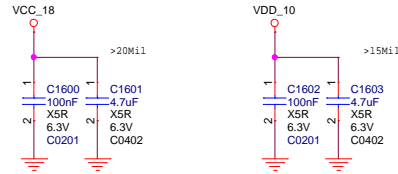
2-Vrms Audio Line Driver

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项目:	EAIK310
文件:	EAIK310_MAINBOARD
图纸:	13.RK3328 AV Interface
修改日期:	Wednesday, May 08, 2019
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设计者:	CZA
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Embed FEPHY

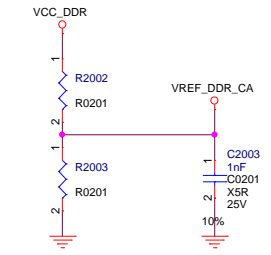
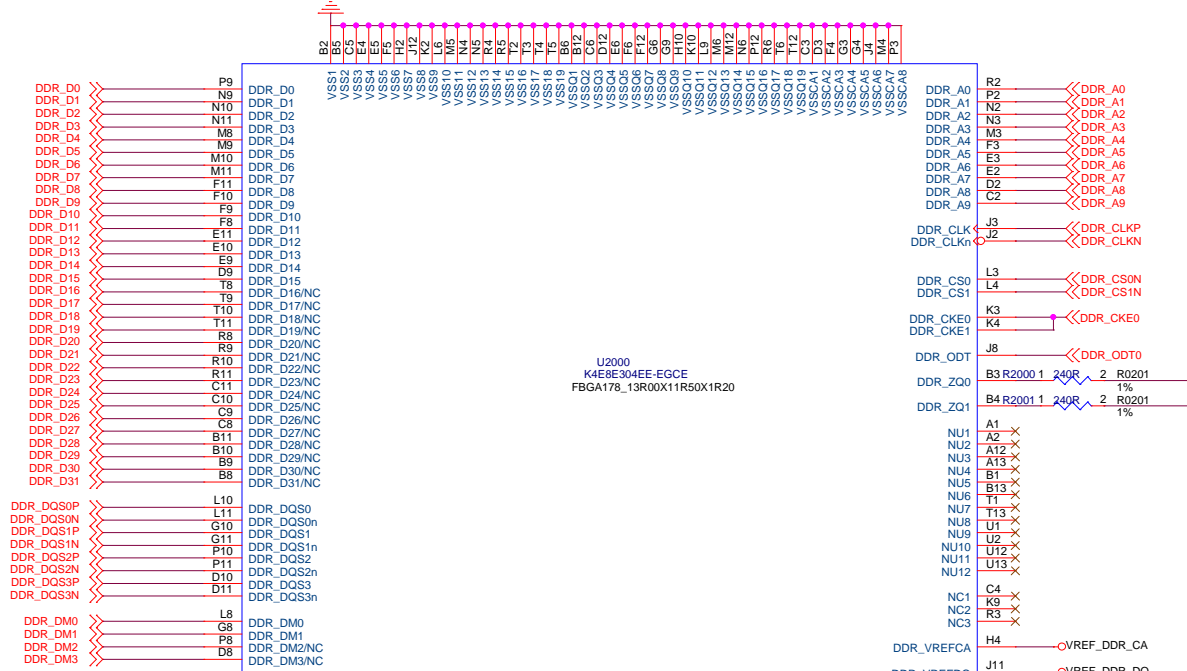


RK3228H
BGA395_14R00X14R00X1R24



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项目:	EAIDK310
文件:	EAIDK310_MAINBOARD
图纸:	14.RK3228 FEPHY
修改日期:	Wednesday, May 08, 2019
设计者:	CZA
版本:	V0.1
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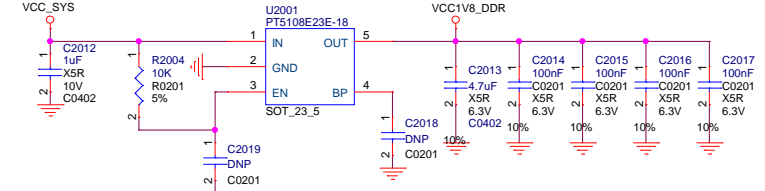
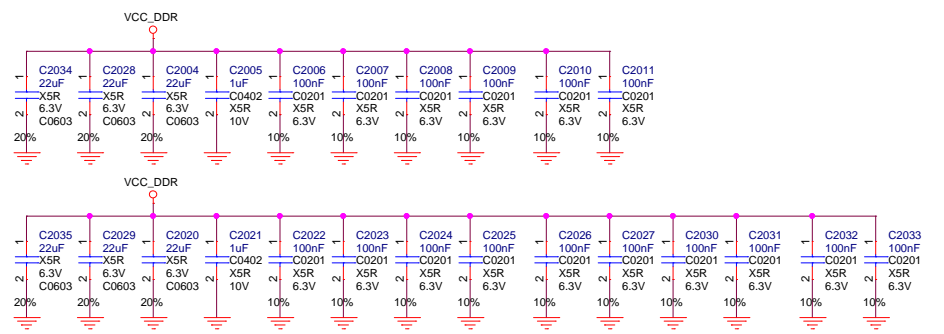
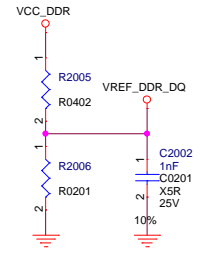
LPDDR3 >=1866Mbps



Symbol	Parameter	Min	Max	Unit	Notes
$V_{DDQ}(AC)$	AC input logic high	$V_{DDQ} \pm 0.150$	Note 2	V	1, 2, 5
$V_{DDQ}(AL)$	AC input logic low	Note 2	$V_{DDQ} \pm 0.150$	V	1, 2, 5
$V_{DDQ}(DC)$	DC input logic high	$V_{DDQ} \pm 0.100$	V_{DDQ}	V	1
$V_{DDQ}(DL)$	DC input logic low	V_{DDQ}	$V_{DDQ} \pm 0.100$	V	1
$V_{REF}(DQ/DQI \text{ enabled})$	Reference Voltage for DQ, DM inputs	$0.42 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	3, 4
$V_{REF}(DQS/DQS0)$	Reference Voltage for DQ, DM inputs	$V_{DDQ} \times 0.4$	$V_{DDQ} \times 0.5$	V	3, 5, 6

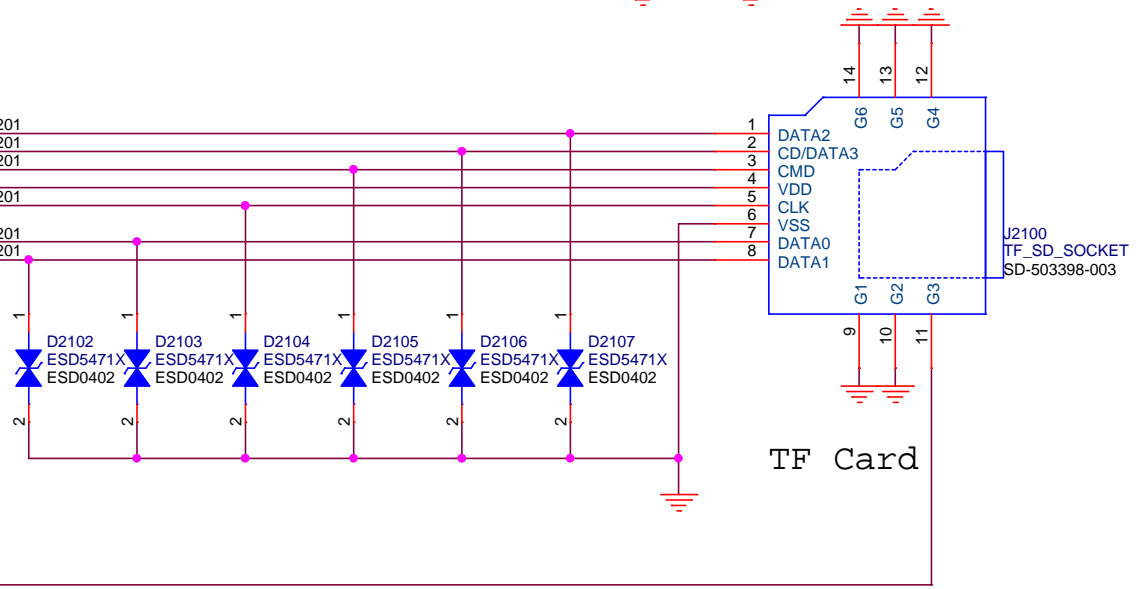
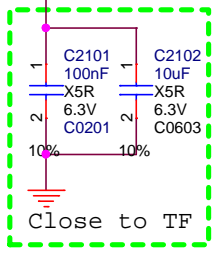
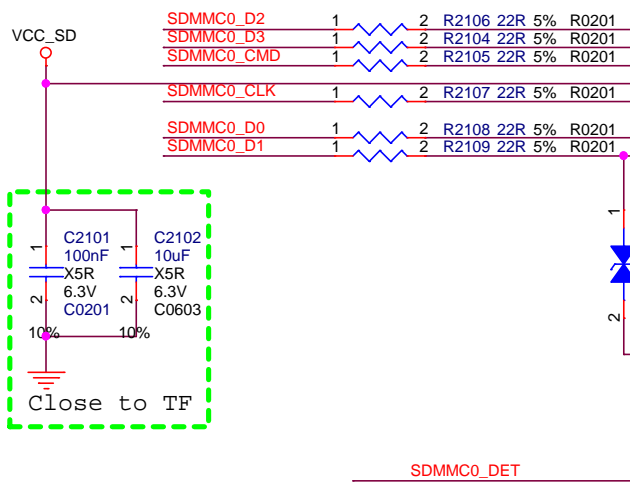
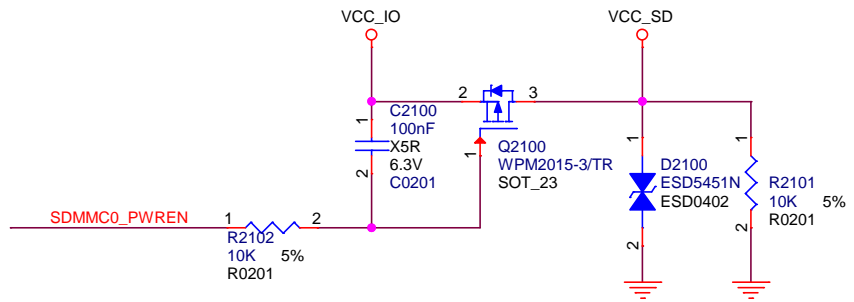
NOTE 1: For DQ input only pins, $V_{REF} = V_{DDQ}/2$.
 NOTE 2: See "Overcurrent and Thermal Shutdown Specifications" on page 69.
 NOTE 3: The signal noise on V_{DDQ} may not allow V_{REF} to deviate from $V_{DDQ}(DC)$ by more than $\pm 15\%$. V_{DDQ} (for reference) approx. ± 12 mV.
 NOTE 4: For reference: approx. $V_{DDQ} \times 2 \pm 12$ mV.
 NOTE 5: For reference: approx. $V_{DDQ} \times 2 \pm 12$ mV.
 NOTE 6: R_{DQ} and R_{DQS} are dimmable register programmed values used for the calculation of $V_{DDQ}(DC)$.

$$V_{REF} = \frac{V_{DDQ} \times (R_{DQ} + R_{DQS})}{R_{DQ} + R_{DQS} + 2 \times V_{DDQ}}$$

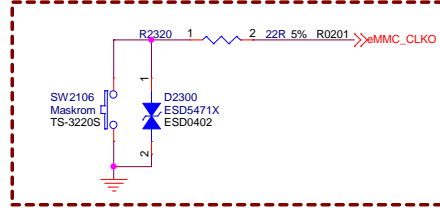
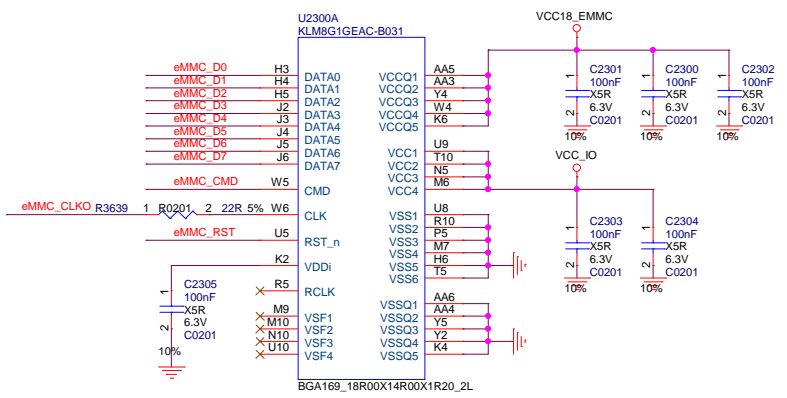
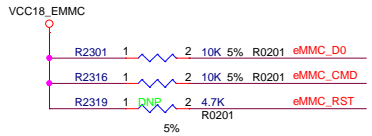


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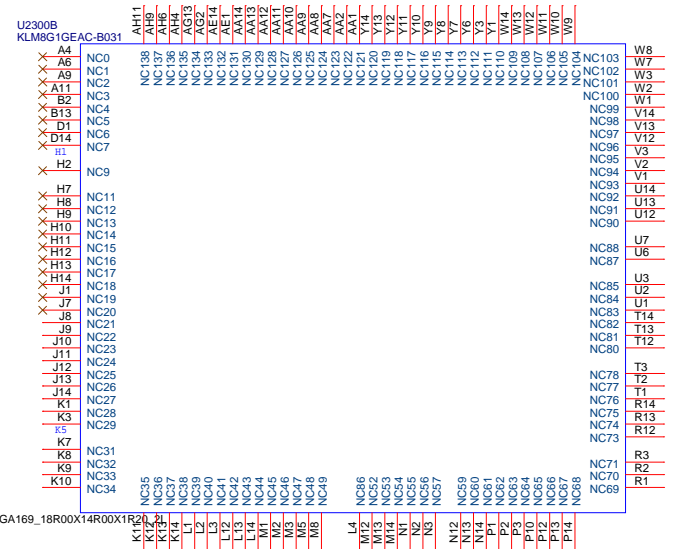
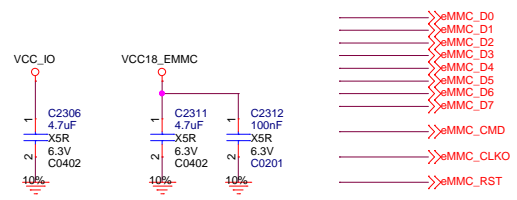
项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图框:	15.RAM LPDDR3_178P		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	15 of 22



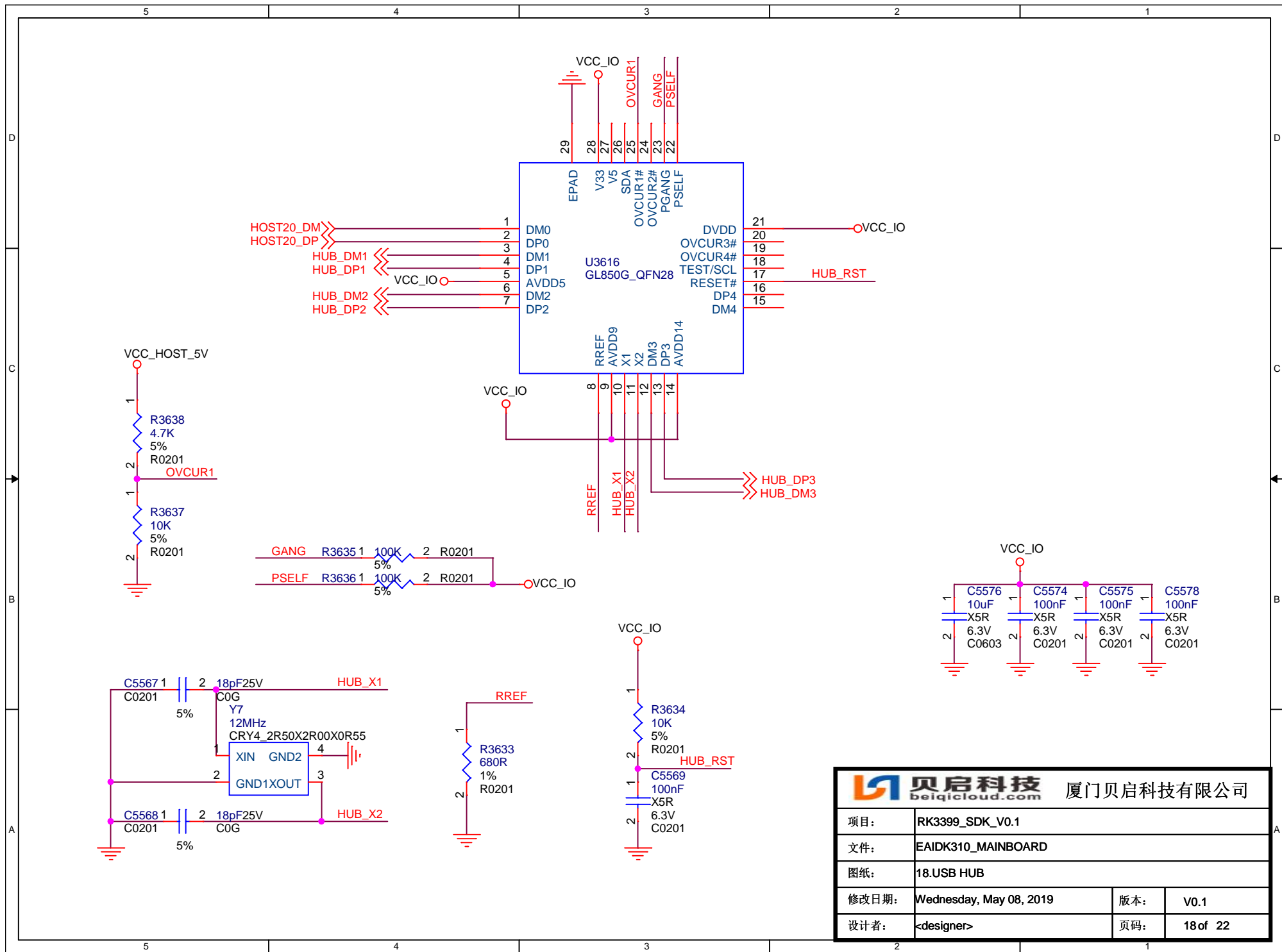
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项目:	EAIK310
文件:	EAIK310_MAINBOARD
图纸:	16.TF/SD Card
修改日期:	Wednesday, May 08, 2019
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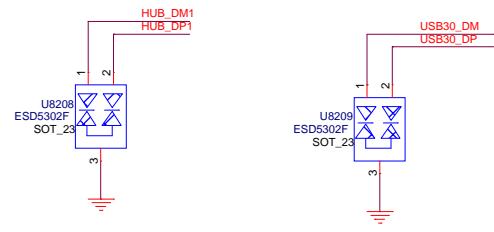
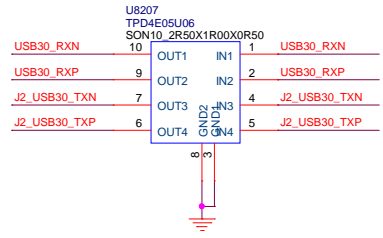
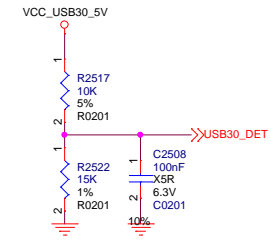
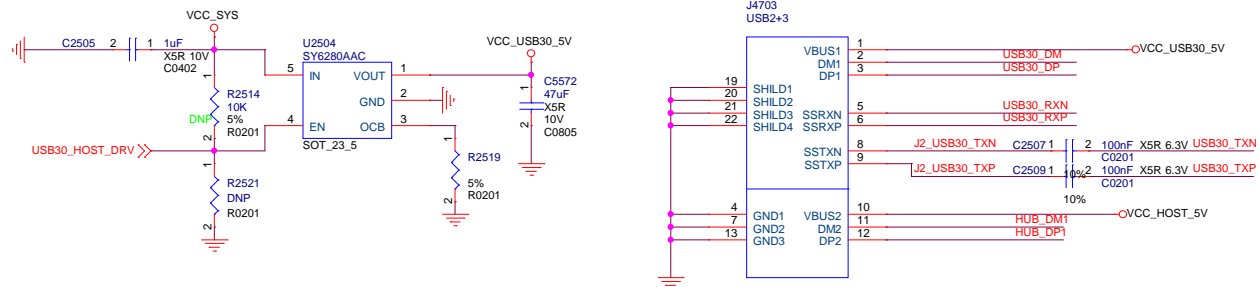
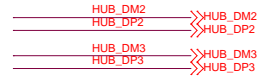
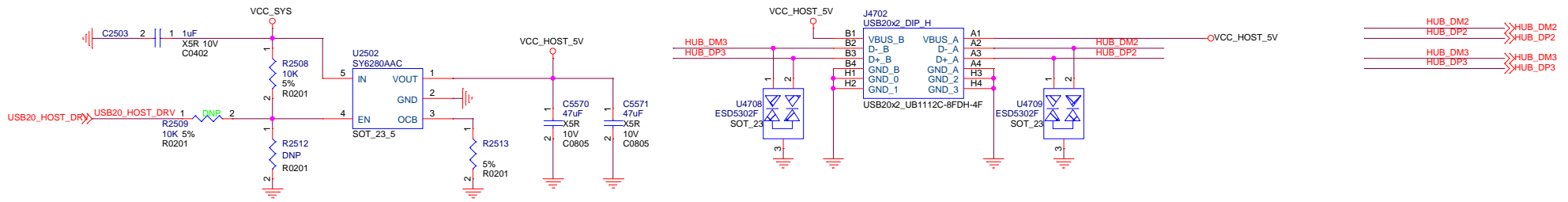
Note:
eMMC Update.



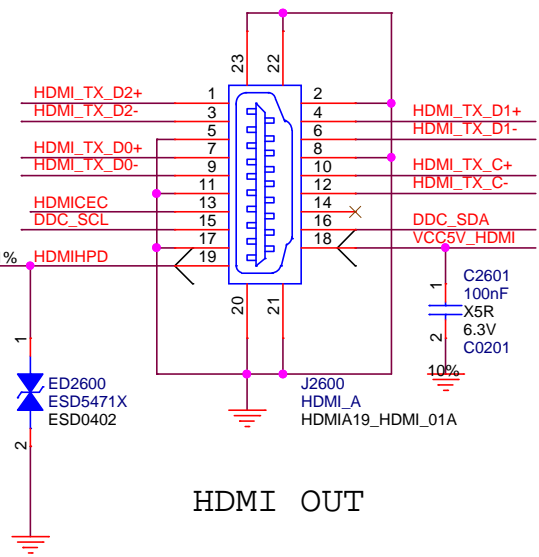
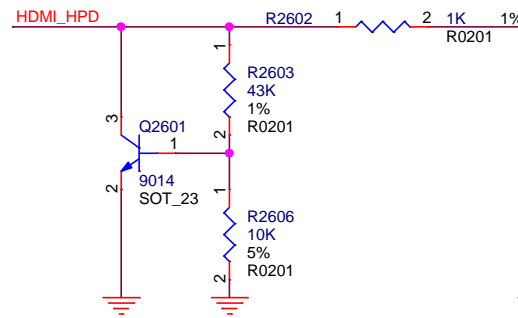
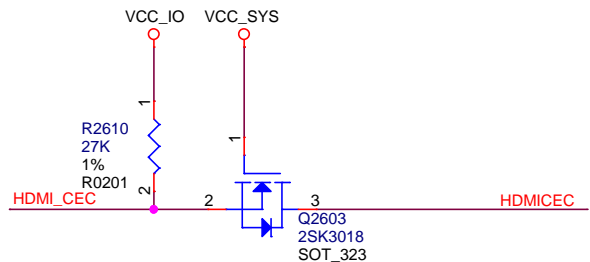
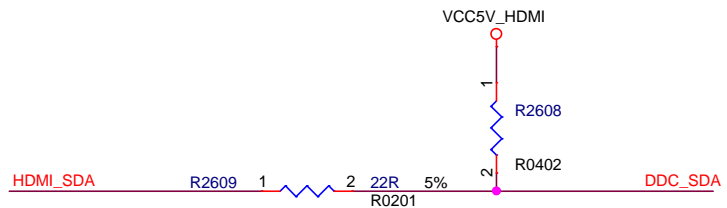
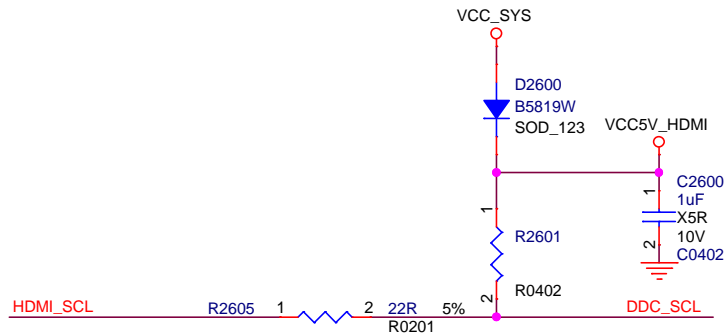
贝启科技 beiqitech.com		厦门贝启科技有限公司	
项目:	EAI DK310		
文件:	EAI DK310_MAINBOARD		
图纸:	17.Flash-eMMC		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	17 of 22



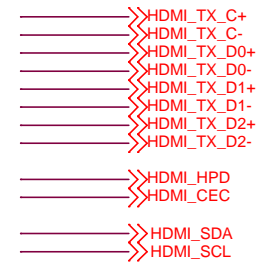
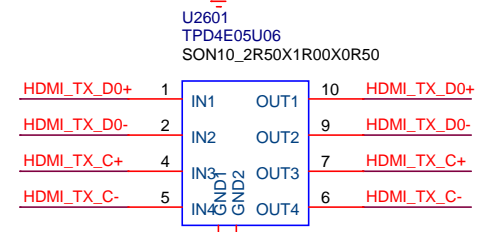
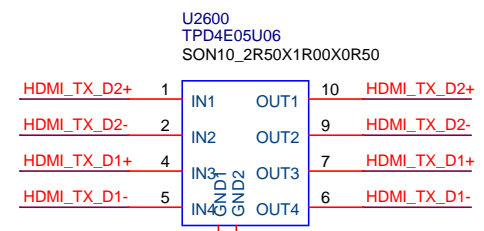
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项目:	RK3399_SDK_V0.1
文件:	EAIDK310_MAINBOARD
图纸:	18.USB HUB
修改日期:	Wednesday, May 08, 2019
设计者:	<designer>
版本:	V0.1
页码:	18 of 22



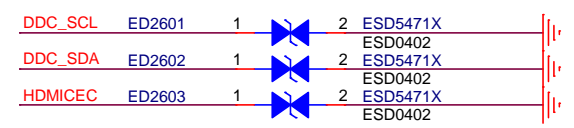
厦门贝启科技有限公司 beiqicloud.com			
项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	19.USB Port		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	19 of 22



HDMI OUT

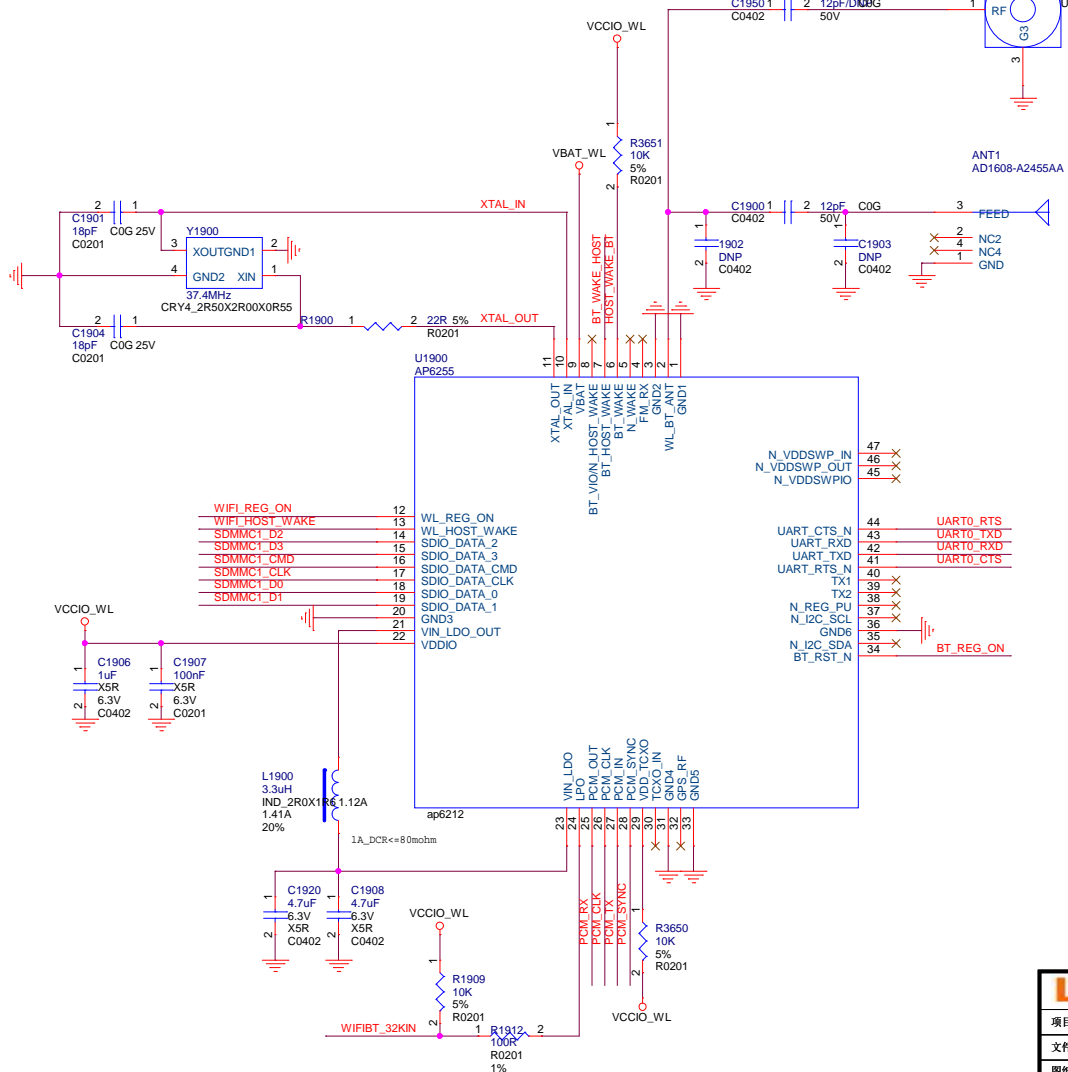
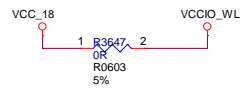
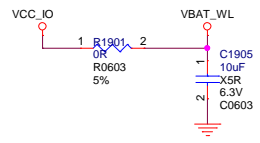
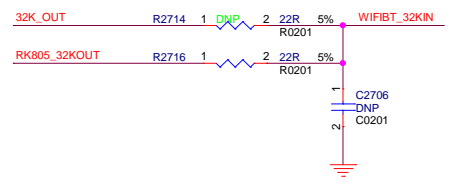


Cj <= 0.4pF

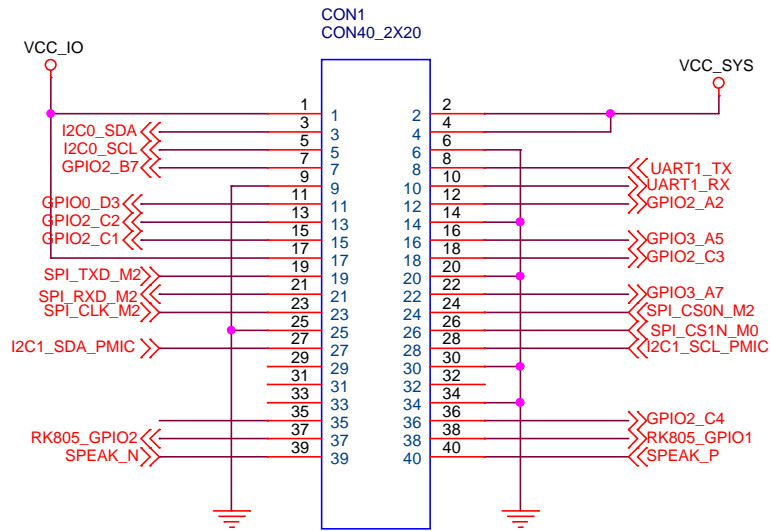


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项目:	EAIDK310		
文件:	EAIDK310_MAINBOARD		
图纸:	20.HDMI OUT Port		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	20 of 22

- PCM_CLK << PCM_CLK
- PCM_SYNC << PCM_SYNC
- PCM_RX << PCM_RX
- PCM_TX << PCM_TX
- PCM_CLK_BT << PCM_CLK_BT
- PCM_SYNC_BT << PCM_SYNC_BT
- PCM_RX_BT << PCM_RX_BT
- PCM_TX_BT << PCM_TX_BT
- BT_WAKE_HOST << BT_WAKE_HOST
- BT_REG_ON << BT_REG_ON
- WIFI_REG_ON << WIFI_REG_ON
- WIFI_HOST_WAKE << WIFI_HOST_WAKE
- RK805_32KOUT << RK805_32KOUT
- 32K_OUT << 32K_OUT
- SDMMC1_D0 << SDMMC1_D0
- SDMMC1_D1 << SDMMC1_D1
- SDMMC1_D2 << SDMMC1_D2
- SDMMC1_D3 << SDMMC1_D3
- SDMMC1_CMD << SDMMC1_CMD
- SDMMC1_CLK << SDMMC1_CLK
- UART0_RTS << UART0_RTS
- UART0_TXD << UART0_TXD
- UART0_RXD << UART0_RXD
- UART0_CTS << UART0_CTS



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项目:	EAIDK310
文件:	EAIDK310_MAINBOARD
图纸:	21.WIFI+BT
修改日期:	Wednesday, May 08, 2019
设计者:	CZA
版本:	V0.1
页码:	21 of 22



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项目:	RK3399_SDK_V0.1		
文件:	EAIDK310_MAINBOARD		
图纸:	22.CONNECTOR		
修改日期:	Wednesday, May 08, 2019	版本:	V0.1
设计者:	CZA	页码:	22 of 22